In the Claims:

1. (Original) A memory device comprising:

a semiconductor substrate;

a first gate insulator on a first portion of a semiconductor substrate;

a storage node on the first gate insulator;

a tunnel junction barrier on the storage node;

a data electrode on the tunnel junction barrier;

a second gate insulator layer on a sidewall of the tunnel junction barrier;

a third gate insulator on a second portion of the substrate adjacent the tunnel junction barrier;

a gate electrode on the second gate insulator and the third gate insulator; and

first and second impurity-doped regions in the substrate coupled by a channel through the first and second portions of the substrate.

2. (Original) A memory device according to Claim 1, wherein the storage node is on a first channel in the first portion of the substrate, and wherein the gate electrode is on a second channel in the second portion of the substrate that couples the first channel to the first impurity-doped region.

3. (Original) A memory device according to Claim 2, wherein the second channel is configured to serve as a source/drain for the first channel.

4. (Original) A memory device according to Claim 1, further comprising a fourth gate insulator on a second sidewall of the tunnel junction barrier and a fifth gate insulator on a third portion of the substrate between the tunnel junction barrier and the second impurity-doped region, and wherein the gate electrode is disposed on the fourth and fifth gate insulators.

5. (Original) A memory device according to Claim 4, wherein the gate electrode is on a third channel region in the third portion of the substrate that couples the first channel to the second impurity-doped region.

6. (Original) A memory device according to Claim 5, wherein the third channel is configured to serve as a source/drain for the first channel.

7. (Original) A memory device according to Claim 4, wherein the second, third, fourth and fifth gate insulators comprise respective portions of a continuous insulation layer conforming to a top of the data electrode and to the sidewalls of the tunnel junction barrier and to surfaces of the substrate adjacent thereto, and wherein the gate electrode comprises a continuous conductive layer overlying the continuous insulation layer.

8. (Original) A memory device according to Claim 7, wherein the gate electrode further comprises conductive sidewall spacers interposed between the portions of the second insulation layer on the sidewalls of the tunnel junction barrier and the continuous conductive layer.

9. (Original) A memory device according to Claim 1, wherein the second and third gate insulators comprise respective portions of a continuous insulation layer conforming to the sidewall of the tunnel junction barrier and to a surface of the second portion of the substrate, and wherein the gate electrode comprises a continuous conductive layer overlying the continuous insulation layer.

10. (Original) A memory device according to Claim 9, wherein the gate electrode further comprises a conductive sidewall spacer interposed between the portion of the second insulation layer on the sidewall of the tunnel junction barrier and the continuous conductive layer.

11. (Original) A memory device according to Claim 10, further comprising an insulation layer on the data electrode, and wherein the gate electrode comprises a portion on the insulation layer on the data electrode.

12. (Original) A memory device according to Claim 10, wherein the gate electrode comprises a continuous conductive layer overlying the second and third gate insulators and the data electrode.

13. (Original) A memory device, comprising:

a semiconductor substrate;

a tunnel junction barrier transistor having a storage node on the substrate, a tunnel junction barrier on the storage node, and a gate electrode on a sidewall of the tunnel junction barrier that controls a channel of the tunnel junction barrier transistor;

a first planar transistor having a first channel in the substrate disposed transverse to the channel of the tunnel junction barrier transistor and controlled by the storage node of the tunnel junction barrier transistor; and

a second planar transistor having a second channel in the substrate disposed adjacent to the first planar transistor and transverse to the channel of the tunnel junction barrier transistor and having a gate electrode electrically coupled to the gate electrode of the tunnel junction barrier transistor.

14. (Original) A memory device according to Claim 13, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a continuous conductive layer having a first portion on the sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto the channel of the second planar transistor.

15. (Original) A memory device according to Claim 13, wherein the second planar transistor comprises second channels on respective sides of the first channel.

16. (Original) A memory device according to Claim 15, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a first continuous conductive layer having a first portion on a first sidewall of the tunnel junction barrier and a second portion that extends transverse to the first portion onto a first one of the second channels of the second planar transistor, and a second continuous conductive layer having a first portion on a second sidewall of the tunnel junction barrier opposite the first sidewall and a second portion that extends transverse to the first portion onto a second one of the second channels of the second planar transistor.

17. (Original) A memory device according to Claim 15, wherein the gate electrodes of the tunnel junction barrier transistor and the second planar transistor comprise a continuous conductive layer disposed on first and second opposing sidewalls of the tunnel junction barrier and on respective portions of the substrate adjacent the first and second sidewalls.

18. (Original) A memory device according to Claim 15, further comprising respective first and second impurity doped regions in the substrate on respective sides of the tunnel junction barrier transistor and electrically coupled to respective ones of the second channels.

19-36. (Canceled)